

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization International Bureau



(43) International Publication Date
13 January 2005 (13.01.2005)

PCT

(10) International Publication Number
WO 2005/004566 A1

(51) International Patent Classification⁷: H05K 3/36, 3/40

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(21) International Application Number:

PCT/SE2003/001183

(22) International Filing Date: 7 July 2003 (07.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (*for all designated States except US*): TELEFONAKTIEBOLAGET LM ERICSSON (publ) [SE/SE]; S-164 83 Stockholm (SE).

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): NILSSON, Mattias [SE/SE]; Örnehufvudsgatan 11, S-412 59 Göteborg (SE). JOHANSSON, Stefan [SE/SE]; Indigogatan 1, S-421 65 Västra Frölunda (SE).

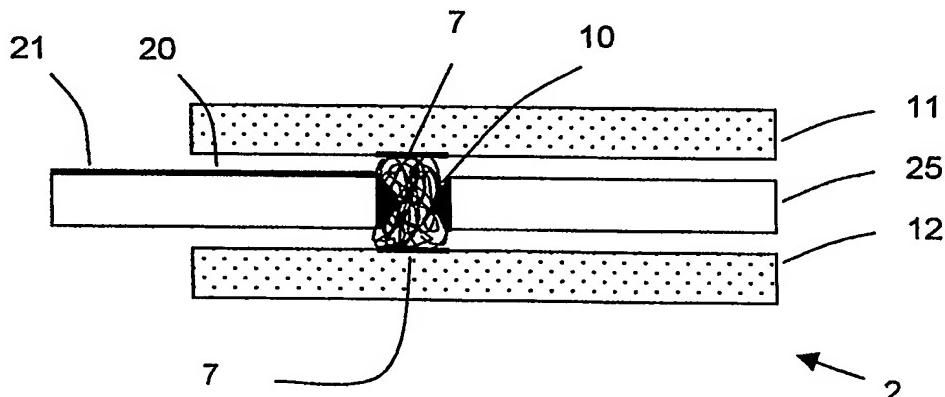
(74) Agent: MOLKER, Anders; Ericsson AB, Patent Unit Radio Networks, S-431 84 Mölndal (SE).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: TESTING OF INTERCONNECTIONS BETWEEN STACKED CIRCUIT BOARDS



(57) Abstract: A retainer board (25, 27, 28) having at least one hole (10) in which a wire button contact (5) is inserted, wherein the hole (10) is plated and at least one conductor (20) is connected to the plated hole for providing outside access. Moreover a method for testing stacked circuit boards are disclosed comprising the steps of detachably arranging at least two circuit boards (11, 12, 29), testing the individual functionality of the circuit boards (11, 12) and if approved, assembling the circuit boards (11, 12) and the first retainer board (25, 27, 28), and asserting whether the overall functionality of the arrangement is approved.

WO 2005/004566 A1